



Jin, B., & Yuan, X. (2019). Topology, Efficiency Analysis and Control of a Four-level π -type Converter. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(2), 1044-1059. [8489873]. <https://doi.org/10.1109/JESTPE.2018.2875485>

Peer reviewed version

License (if available):
Other

Link to published version (if available):
[10.1109/JESTPE.2018.2875485](https://doi.org/10.1109/JESTPE.2018.2875485)

[Link to publication record in Explore Bristol Research](#)
PDF-document

This is the accepted author manuscript (AAM). The final published version (version of record) is available online via IEEE at <https://doi.org/10.1109/JESTPE.2018.2875485> . Please refer to any applicable terms of use of the publisher.

University of Bristol - Explore Bristol Research

General rights

This document is made available in accordance with publisher policies. Please cite only the published version using the reference above. Full terms of use are available:
<http://www.bristol.ac.uk/red/research-policy/pure/user-guides/ebr-terms/>

Topology, Efficiency Analysis and Control of a Four-level π -type Converter

Bosen Jin, Xibo Yuan, *Senior Member, IEEE*

Abstract—This paper provides a comprehensive analysis for a four-level π -type converter for low-voltage applications. This topology is a kind of reduced device-count neutral point clamped multilevel converter, and formed by only six switches in each phase leg. The line (phase-to-phase) output voltage can have seven levels and the output harmonics are much lower than that of a standard two-level converter. The switching states and their associated output voltage levels have been analyzed. A generalized averaged analytical power loss model of this converter has also been developed to investigate the loss distribution among the power devices as well as the efficiency. The four-level π -type converter has a higher efficiency when the switching frequency is above 5 kHz compared with two-level and three-level converters with the power devices used in this paper. The reduced output harmonics, hence reduced filtering requirement together with improved efficiency hence reduced cooling (heatsink) requirement offer a higher density alternative to the two-level converter. A simplified level shifted carrier-based modulation method with dynamic optimal zero-sequence signal injection has been employed to modulate the converter and to control dc-link neutral points' voltages. This paper has experimentally validated the predicted four-level π -type converter efficiency and the neutral point voltage balancing control with a back-to-back configuration under high modulation indices and unity power factor. The neutral point voltage balance region has been plotted and experimentally verified.

Index Terms—Multilevel converter, four-level converter, pulse width modulation, low voltage application, power loss, voltage balancing control.

I. INTRODUCTION

MULTILEVEL converters are default candidates in medium-voltage (3~33kV), high-power applications. Nevertheless, they are also considered for low-voltage (200~460V) applications as an alternative to the conventional two-level converter to achieve higher power density [1]. Converter topologies that can generate output phase voltages of more than three levels, such as four-level converters [2-4] or five-level converters [5-7] have been studied. To achieve

equivalent output harmonics, the switching frequency of multilevel converters can be kept low when compared to a two-level converter, consequently reducing switching losses and shrinking the heatsink size. On the other hand, if operated at the same switching frequency, the filter size of multilevel converters can be smaller. Either way will improve the system power density, which is desired in applications such as more electric aircraft, electric/hybrid vehicles and renewable power generation, where the converter volume and weight is an important factor. In addition, compared to the two-level converter, multilevel converters have a lower switching voltage, i.e. a portion of the dc-link voltage rather than the full dc-link voltage [8], resulting in a lower switching loss. This means the converter efficiency drops slowly with the increase of the switching frequency [9], which provides the possibility to further increase the switching frequency and achieve a higher power density.

Although the output harmonics can be further reduced with converters of higher number of voltage levels, the main concern is the increased complexity regarding the circuit and control [4]. According to the derivation principles for multilevel converters with reduced device count [10-14], an active neutral point clamped four-level π -type converter was introduced with only six switching devices per phase leg [15-17]. Compared with other four-level converters or even five-level converters, there are no clamping diodes or flying capacitors as required in a diode neutral-point-clamped (NPC) converter or a flying capacitor (FC) converter, and less total switching devices count, which simplifies the circuitry, reduces the total conduction loss and is suitable for low-voltage applications. This further makes the four-level π -type converter be beneficial for high-density applications such as aerospace systems and EV systems. However, there are no existing detailed control and performance analysis for this topology. Given the power loss of each switching device is different, an effective loss model needs to be developed to quantitatively assess the loss distribution of the π -type converter as well as efficiency against the two-level and three-level converters. An analytical loss model derived based on the averaged power loss over one fundamental cycle can directly reveal the relationship between the power loss and system parameters such as voltage, current, power factor, modulation index, etc and it is computationally efficient [1, 8]. This paper has developed a generalized analytical power loss model for the four-level π -type converter, which can be used to evaluate the device power loss and converter efficiency under

Manuscript submitted December 10, 2017; revised July 23, 2018; accepted October 03, 2018. Date of current version October 07, 2018. This work was supported by the UK EPSRC under Grant EP/K035096/1 and Grant EP/R004137/1. Corresponding author: Xibo Yuan.

B. Jin, X. Yuan are with the Department of Electrical and Electronic Engineering, University of Bristol, Bristol BS8 1UB, United Kingdom. (e-mail: bosen.jin@bristol.ac.uk; xibo.yuan@bristol.ac.uk).

various modulation indices, power factors and switching frequencies. With calculation based on the developed loss model, it has been found out that the four-level π -type converter can have higher efficiency at switching frequencies above 5 kHz compared with the two-level or three-level converters due to the lower switching voltage.

A challenging issue for neutral point clamped multilevel converters is the balancing of the dc-link capacitors' voltages (neutral point voltages) [4], [18-23]. The voltage drift in neutral points may affect the system stability as well as the output harmonics. Active neutral point voltage control methods have been researched in [18, 19], [21-33]. Control methods based on a virtual vector PWM (VV PWM) can achieve the dc-link capacitor voltage balance with a passive front-end for a four-level converter or even n-level converters under any power factors and modulation indices [28-31]. However, the switching pattern for each phase in each switching period involves more than two voltage levels, and switching actions are doubled. This increases switching losses as well as the output harmonics. In addition, the carrier-based implementation of VV PWM is relatively computationally intensive. For an n-level converter, it requires n-1 modulation waves in each phase, and corresponding offsets to each modulation wave have to be calculated according to the requirements specifically [24, 36]. The conventional nearest-three-vectors PWM (NTV PWM) for the diode-NPC four-level converter can optimize the switching loss and the total harmonic distortion (THD) [4, 22, 23, 27, 32, 33] and in each switching period only two voltage levels are used and there are only two switching actions. The carrier-based implementation of the NTV PWM can be realized by injecting appropriate zero-sequence signals to the sinusoidal modulation wave of each phase [6, 17, 21, 25, 26, 34-38], which is relatively easy to implement compared to the VV PWM. However, this method cannot guarantee the neutral point voltage balance at high modulation indices and high power factors, if a passive front end rectifier is used [4, 22, 23, 27, 32, 33]. This problem can be overcome if a back-to-back structure with an active front end is used [6, 17, 19, 21-23, 27, 33]. Even though, when both sides operate at different modulation indices under high power factors (unity power factor as an extreme), the dc-link capacitor voltage balance still cannot be guaranteed at all the operating points [25-27, 39]. Experimental control of a back-to-back five-level NPC converter based on the NTV PWM is given in [22, 23, 27]. The method which coordinates power angles of both rectifier and inverter sides with offline modulation wave calculation has been experimentally verified in [6, 21], which may not be practical in real applications. [39] addresses the control limits of back-to-back three-level NPC converters for eliminating the neutral point voltage ripple. The control limits of back-to-back five-level diode-NPC converters have been given in [25, 26] with offline-calculated modulation signals by simulations. [27] validated the back-to-back five-level diode-NPC converter control limits by the NTV PWM, focusing on the impact of power factors.

The contributions of this paper are summarized as follows. It extends the work in [9, 17, 38] and addresses the efficiency and control aspects of the four-level π -type converter. It

provides additional experimental efficiency, harmonic comparison between the two-level converter and the four-level π -type converter. A simplified level shifted (LS) carrier-based modulation with dynamic optimal zero-sequence injection for dc-link neutral point voltage balancing control has been employed for the four-level π -type converter. This paper also demonstrates in experiment a back-to-back four-level π -type converter successfully balancing dc-link neutral point voltages with the proposed modulation and control strategy under unity power factor and various modulation indices. A dc-link capacitor voltage balanceable region for the back-to-back four-level π -type configuration with various modulation indices on both sides has been given and experimentally verified as well.

This paper is organized as follows. Section II introduces the topology and the switching states of the four-level π -type converter. Section III presents the averaged analytical power loss model of the four-level π -type converter. Section IV presents a LS carrier-based dc-link neutral point voltage balancing control method. Section V presents the power loss analysis results as well as the experimentally-measured converter efficiency. The back-to-back configuration with dc-link capacitor voltage balancing control has been experimentally verified as well. Finally, Section VI concludes the paper.

II. CONVERTER TOPOLOGY AND SWITCHING STATES

Fig.1 (a) shows a phase-leg structure of the four-level π -type converter, which has six switching devices. T1 and T6 are the same as in a conventional two-level converter and required to block the whole dc-link voltage. Hence, for low voltage applications, e.g. dc-link voltage $V_{dc}=600V$, T1 and T6 will usually be 1200V devices such as IGBTs in order to leave enough voltage margin. The dc-link neutral points N1 and N2 are connected to the converter phase leg output through two bidirectional neutral paths. These two neutral paths are created by two pairs of IGBTs (T2, T3 and T4, T5), connected back-to-back respectively. In Fig.1 (a), T3 and T4 need to withstand $2/3$ of the dc-link voltage ($2E$). T2 and T5 only need to withstand $1/3$ of the dc-link voltage (E). Therefore, for a $V_{dc}=600V$ application, T2 ~ T5 can be implemented with 600V IGBTs. With this configuration, the phase leg can output four voltage levels. And three phase legs can form a three-phase converter.

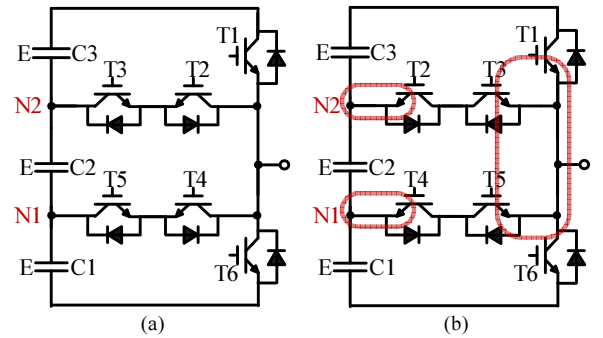


Fig.1. A four-level π -type converter phase leg: (a) with common emitter connection of IGBTs as neutral paths, (b) with common collector connection of IGBTs as neutral paths.

Although the four-level π -type converter has more components than a two-level converter, it only requires 6 switching devices per phase leg, which is a minimum for a four-level converter, without any clamping diodes or flying capacitors as in other topologies. Also, it has less dv/dt , less EMI, smaller filter requirement and higher efficiency (smaller heatsink), which will offset the device count aspect. Meanwhile, in terms of the number of required gate driver power supplies, as shown in Fig.1 (a), T2 and T3, with common emitter connection can share the same gate drive power supply, so as for T5 and T4. Therefore, 6 additional isolated gate driver power supplies are required for a three-phase four-level π -type converter compared with the two-level converter. This number can be further reduced when the two back-to-back IGBTs are connected in a common collector configuration as shown in Fig.1 (b). T1, T3 and T5 can share the same gate driver power supply. The emitters of T2 and T4 connect to the two neutral points N1 and N2 respectively. Thus, T2 and T4 will need two separate gate power supplies, which can be shared by all the three phase legs. In total, only two additional gate power supplies are needed for a three-phase four-level π -type converter.

Meanwhile, compared with some other four-level converters, the four-level π -type converter has the minimum total number of devices. Table I shows the comparison between various four-level converter topologies.

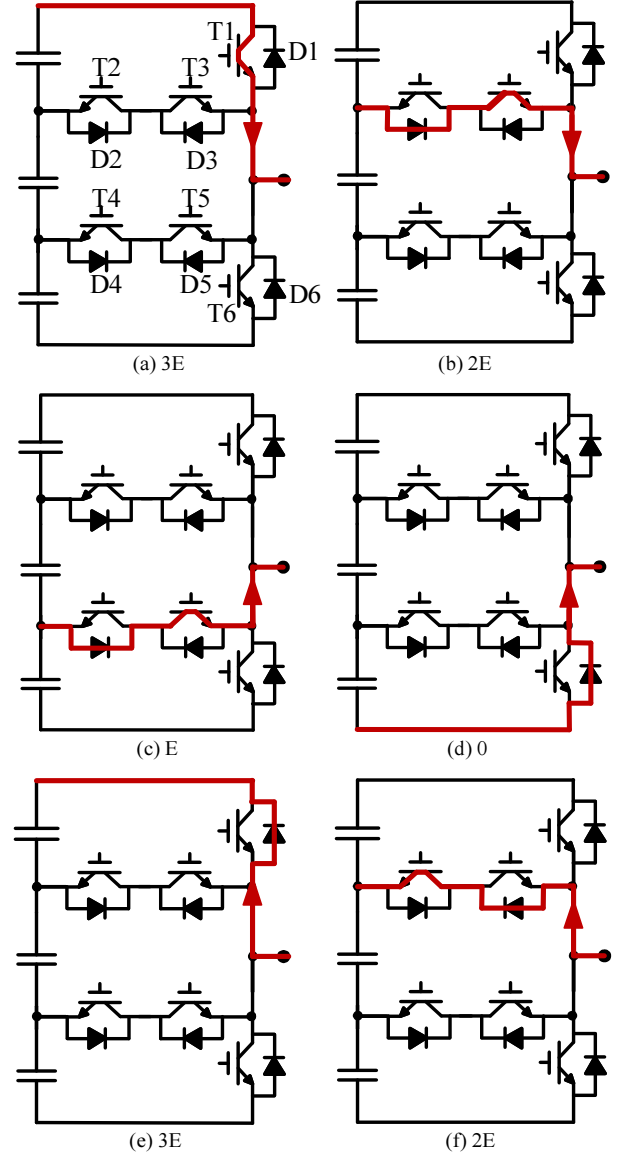
TABLE I COMPARISON OF FOUR-LEVEL CONVERTERS (PHASE LEG)

Topology	Device switching voltage (V)	Single-end dc-link capacitors voltage balancing capability	NO. of switching devices per phase leg	NO. of FCs
Four-level π -type converter	$V_{dc}/3$	No	6	N/A
FC four-level converter	$V_{dc}/3$	Yes	6	3
NPC four-level converter	$V_{dc}/3$	No	6 + 4 clamping diodes	N/A

Regarding efficiency and power losses, as all the four-level converters switches in a very similar manner, e.g. only switching a portion ($1/3$) of the dc-link voltage, the switching loss is very similar. Regarding conduction loss, as the π -type converter only has one device in conduction for two (highest and lowest levels) of the four output voltage levels, it has a slightly lower conduction loss. Overall, the efficiency between various four-level converters are very similar. Regarding output harmonics, as all the four-level converters output four levels in the phase voltage and seven levels in the line voltage, their harmonics are almost the same.

The π -type converter output voltage levels as well as corresponding switching states according to the current direction are shown in Fig.2. In order to guarantee successful commutations from one level to an adjacent level for the purpose of reducing the voltage stress of each device, especially during the dead-time period, one device must be kept "ON" during both the two voltage levels. For example, switching from 3E to 2E when the current flows out of the inverter as shown in

Fig.2 (a) (b), T3 should be always "ON". In this case, T1 and T2 switch ON and OFF in a complementary manner. T1 is turned ON to output 3E voltage, where the current flows through T1. While T2 is turned ON to output 2E voltage, where the current flows through D2 and T3. During dead-time, T1 and T2 are both "OFF", where the current flows through D2 and T3 as well. Therefore, T1 and T2, T3 and T4, T5 and T6 switch in a complementary manner. This can be realized by a LS carrier-based modulation strategy as shown in Fig.3. The intersection of the modulation wave and each carrier wave determines switching states of one pair of switching devices. It should be noted that since the output voltage only switches between adjacent voltage levels with one voltage step (E, a third of the dc-link voltage), the switching voltage for each device (T1~T6) is E (e.g. 200V for a 600V dc-link voltage). Due to the reduced switching voltage for all the switching devices, the switching loss of the converter is reduced. In contrast, all the devices of the conventional two-level converter have to switch the full dc-link voltage which leads to a higher switching loss.



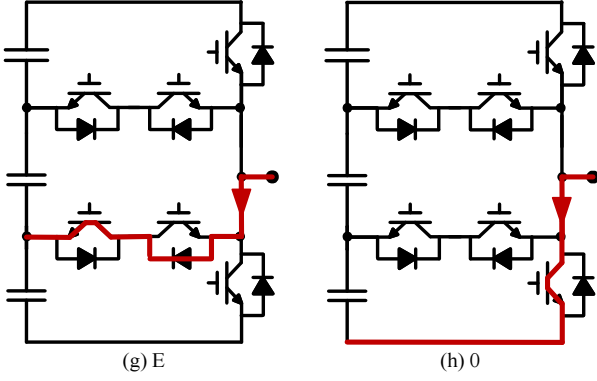
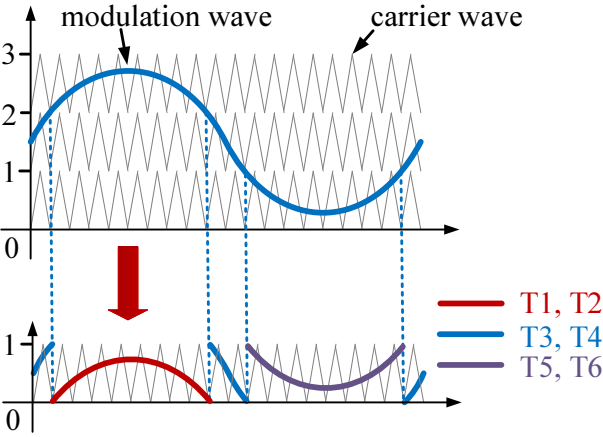


Fig.2. Switching states and current flow paths

Fig.3. Level shift carrier-based modulation scheme for the four-level π -type converter.

III. CONVERTER POWER LOSS MODEL

In contrast to the two-level converter where power losses are concentrated in the two devices in the phase leg, power losses of a four-level π -type converter are distributed among the six devices. Hence, the thermal stress of each device can be lower. Therefore, power loss analysis will be useful to assess this. In this section, the average analytical power loss model of the converter has been established to investigate how power losses are distributed among devices within the four-level π -type converter. Generally, the power loss of a switching device includes the conduction loss as well as the switching loss during the turn-on and turn-off process.

A. Conduction Loss

Conduction losses occur when a device is at ON-state and the current flows through it. Therefore, the instantaneous conduction power loss can be expressed as the ON-state voltage drop multiplied by the ON-state current as shown in (1).

$$P_{con} = v_{CE} |i_c| \quad (1)$$

$$v_{CE} = V_{CE0} + \frac{V_{CEN} - V_{CE0}}{I_{CN}} |i_c| = V_{CE0} + r_0 \cdot |i_c| \quad (2)$$

where, v_{CE} is the switching device voltage drop. V_{CE0} represents the equivalent IGBT on-state threshold voltage. V_{CEN} is the

switching device voltage drop at the rated current. r_0 represents the IGBT equivalent ON resistance. i_c is the IGBT collector current or diode forward current and I_{CN} is the rated current for the switching device. With sinusoidal current, the average conduction loss over one fundamental cycle can be expressed as an integration formula in (3) by combining (1) and (2).

$$P_{con} = \frac{1}{2\pi} \int_{\theta_1}^{\theta_2} k \left[V_{CE0} \cdot |I_{CM} \sin(\omega t - \varphi)| + r_0 \cdot (I_{CM} \sin(\omega t - \varphi))^2 \right] d\omega t \quad (3)$$

where I_{CM} is the load peak current. φ is the power factor angle. k is the ON-state ratio which represents the device conducting duty cycle. θ_2, θ_1 are integration boundaries depending on the conduction interval of the device in the corresponding operation area. Due to the circuit configuration and carrier-based modulation method being used, the ON-state ratio k in (3) has different expressions in various regions which are summarized in Table II using the method in [40].

TABLE II. ON-STATE RATIO WITH DIFFERENT REGIONS

Region	Switching State	k (on-state ratio)
P ~ O+	P	$-\frac{1}{2} + \frac{3}{2} m \cdot \sin(\omega t)$
	O+	$\frac{3}{2} - \frac{3}{2} m \cdot \sin(\omega t)$
O+ ~ O-	O+	$\frac{1}{2} + \frac{3}{2} m \cdot \sin(\omega t)$
	O-	$\frac{1}{2} - \frac{3}{2} m \cdot \sin(\omega t)$
O- ~ N	O-	$\frac{3}{2} + \frac{3}{2} m \cdot \sin(\omega t)$
	N	$-\frac{1}{2} - \frac{3}{2} m \cdot \sin(\omega t)$

Fig.4 presents conduction intervals of switching devices in relation to the fundamental output phase voltage v_p (with reference to the middle point of the dc-link) and load current i_c for the four-level π -type converter when an inductive load is used. Different modulation indices m and power factors angle φ will lead to different conduction intervals as shown in Fig.4 (a)-(d) respectively. For example, in Fig. 4 (a) (b), the various relationships between the power factor angle φ and the voltage level divided angle $\sin^{-1}(\frac{1}{3m})$ lead to different conduction intervals for each device. Consequently, the integration boundary θ_2, θ_1 in (3) can be obtained from there. The complete conduction intervals for each device are given in the Appendix of this paper. In Table II and Fig.4, the switching state P means T1 is ON and the inverter output phase voltage v_p equals to $3E/2$. Note here, the reference voltage is chosen as the mid-point of the dc-link. O+ denotes T2 and T3 are ON, and $v_p = E/2$; O- indicates T4 and T5 are ON and $v_p = -E/2$ while N means T6 is ON and $v_p = -3E/2$, where $3E$ is the total dc-link voltage.

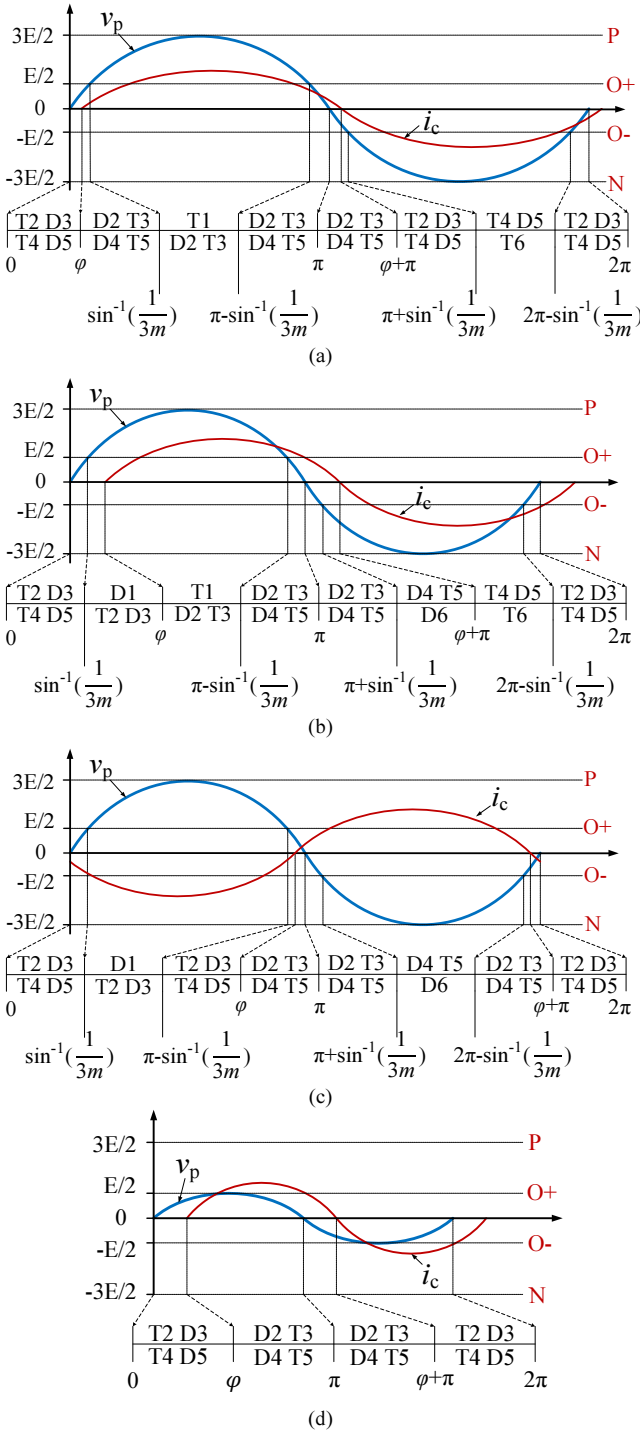


Fig.4. Conduction intervals for switching devices

(a) $m > \frac{1}{3}$, $\varphi \leq \sin^{-1}(\frac{1}{3m})$. (b) $m > \frac{1}{3}$, $\sin^{-1}(\frac{1}{3m}) < \varphi < \pi - \sin^{-1}(\frac{1}{3m})$. (c) $m > \frac{1}{3}$, $\pi - \sin^{-1}(\frac{1}{3m}) \leq \varphi < \pi$. (d) $m \leq \frac{1}{3}$.

B. Switching Loss

The total switching loss consists of turn-on loss and turn-off loss. For anti-parallel diodes, the reverse recovery loss is considered. The switching energy can be modelled as in (4), where the switching energy is assumed to be proportional to the switching voltage (V_{sw}) and have a quadratic relationship with the current [41].

$$E_{sw} = (A_0 + B_0 \cdot |i_c| + C_0 \cdot i_c^2) \frac{V_{sw}}{V_{base}} \quad (4)$$

where, V_{sw} is the switching voltage of the power device. V_{base} is the reference voltage used for characterizing the switching energy in the device datasheet. V_{sw}/V_{base} is included assuming the device switching energy is proportional to the device switching voltage. A_0 , B_0 , C_0 are coefficients describing the relationship between the switching energy and the current which can be found through curve fitting the switching energy given in the datasheet [42, 43]. Switching energy curves are different for IGBT turn-on, turn-off and diode reverse recovery. The switching loss can be generally expressed as

$$P_{sw} = \frac{f_c}{2\pi} \cdot \frac{V_{sw}}{V_{base}} \int_{\theta_1}^{\theta_2} \left[A_0 + B_0 \cdot |I_{CM} \sin(\omega t - \varphi)| + C_0 \cdot (I_{CM} \sin(\omega t - \varphi))^2 \right] d\omega t \quad (5)$$

Here, f_c is the carrier (switching) frequency, and the switching loss is a function of carrier frequency, peak current and power factor. Note that integration boundaries θ_2 , θ_1 in (5) depend on device switching intervals within the corresponding operation area. They are not the same as boundaries in (3). Switching intervals for each device are given in the Appendix. Power loss calculation results for the four-level π -type converter according to the method given above will be presented in part A of Section V.

It should be noted that all the device parameters from the datasheet used here for calculation were based on the worst case (175°C junction temperature), and did not consider parasitic effects. This will provide a quick estimation for the converter thermal performance based on the datasheet information. If the temperature and parasitic effects for a specific prototype need to be considered, additional experimental measurements are needed, e.g. through double-pulse tests once the converter prototype has been built.

The derivation of the presented loss model is a generalized method. Currently, it is based on the sinusoidal modulation. If any pre-calculated zero-sequence components need to be injected to the sinusoidal waveform, e.g. to fully utilize the dc-link voltage, etc, the fundamental phase voltage v_p in Fig.4 can be changed accordingly to reflect their impact on the power loss. Consequently, the corresponding conduction intervals as well as switching intervals in Appendix will be changed accordingly.

IV. MODULATION AND CONTROL STRATEGY

Similar as other four-level converters, the π -type converter has the issue of balancing the three dc-link capacitors (neutral points) voltages, especially the voltage of the middle capacitor C2 in Fig.1. Fig.5 illustrates the charging and discharging conditions of C2 over one fundamental cycle under sinusoidal operations for two extreme conditions, i.e. with unity power factor and zero power factor. Here, a staircase output voltage waveform is used instead of PWM output voltage to simplify the analysis. When the output voltage equals to $E/2$ or $-E/2$, the load current will flow through the capacitor C2 causing its charge and discharge depending on the current direction. As

seen, with unity power factor, where the voltage and current are in phase, in one fundamental period, C2 keeps discharging (current flows out of C2) during output voltage levels of $E/2$ and $-E/2$. As a result, the capacitor C2 voltage will eventually discharge to zero. In contrast, when the load power factor is 0, where the voltage and current have a 90-degree phase shift, in one fundamental period, the charge and discharge of C2 is balanced. Therefore, it is harder to balance the dc-link capacitor voltages at high power factors. Also, at high modulation indices, capacitor voltages are more difficult to balance due to the limited choice of redundant switching states or zero-sequence voltage [4]. In the following, a LS carrier-based modulation with dynamic zero-sequence voltage injection is presented to regulate capacitor voltages.

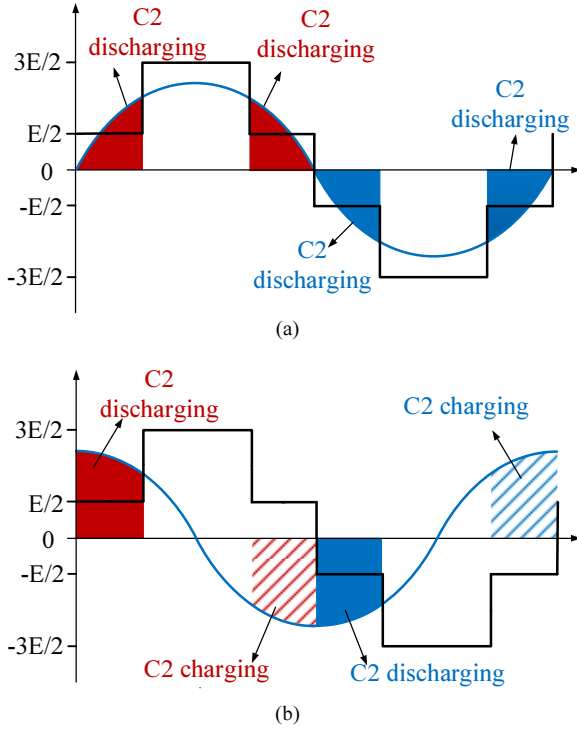


Fig.5. Charge and discharge conditions of C2 (a) power factor=1, (b) power factor=0.

The reference voltage (modulation wave) for the converter is composed of two parts: fundamental components (three-phase sinusoidal) and a zero-sequence component as given in (6).

$$u_i(t) = u_i^*(t) + c(t) \quad i = a, b, c \quad (6)$$

where, $u_i(t)$ is the reference voltage; $u_i^*(t)$ is the fundamental component; $c(t)$ is the zero-sequence component. The fundamental component can be obtained through the output of the current control loop, which are used to regulate the fundamental current of the converter in order to track the reference value. The zero-sequence component can be adjusted and added to the three-phase fundamental components simultaneously to achieve the neutral point voltages balancing.

Due to the LS carrier-based modulation scheme used for the control as shown in Fig. 3, the phase reference voltage can be normalized with 1/3 of the dc-link voltage (e.g. E in Fig.1) and

then the per unit value of the phase reference voltage with regards to the negative dc-bus will be in the range of 0~3. In order to guarantee the converter operating without overmodulation, the maximum and minimum zero-sequence component $c(t)$ that can be injected to fundamental components can be expressed as

$$-u_{\min}^*(t) \leq c(t) \leq 3 - u_{\max}^*(t) \quad (7)$$

where, u_{\max}^* and u_{\min}^* are the maximum and minimum value of the three-phase fundamental components, which are given by

$$\begin{cases} u_{\min}^*(t) = \min(u_a^*(t), u_b^*(t), u_c^*(t)) \\ u_{\max}^*(t) = \max(u_a^*(t), u_b^*(t), u_c^*(t)) \end{cases} \quad (8)$$

After the available range of zero-sequence signal $c(t)$ is derived by (7), the optimized zero-sequence signal can be selected from it according to an appropriate cost function. During each sampling period (switching period) several values within the range given in (7) can be sampled. For example, ten values of the zero-sequence signal can be selected evenly within the range given in (7) and evaluated against the control objective function within each switching period. And the one which leads to the optimized value of the control objective function will be selected. To balance dc-link capacitors' voltages, the control objective can be set to minimize the capacitor energy variation J , and the objective function can be expressed as in (9) [19, 33, 44].

$$J = \frac{1}{2} C \sum_{j=1}^3 \Delta v_{Cj}^2 = \frac{1}{2} C \sum_{j=1}^3 (v_{Cj} - \frac{V_{dc}}{3})^2 \quad (9)$$

where, Δv_{Cj} is the voltage deviation of capacitor C_j in Fig.1(a) from 1/3 of the dc-link voltage. v_{Cj} is the capacitor voltage. V_{dc} is total the dc-link voltage. C is the capacitor value. As the quadratic function J is positive defined, thus, if an optimized zero-sequence signal is selected, J can be minimized (towards zero) when capacitor voltages are regulated at the reference value of 1/3 of the total dc-link voltage. Consequently, when J is minimized, the derivative of J becomes negative or zero as shown in (10).

$$\frac{dJ}{dt} = C \sum_{j=1}^3 \Delta v_{Cj} \frac{dv_{Cj}}{dt} = \sum_{j=1}^3 \Delta v_{Cj} i_{Cj} \leq 0 \quad (10)$$

where, i_{Cj} is the current flowing through the capacitor C_j . This expression can link the control objective to dc-link capacitor currents i_{Cj} . Therefore, the control objective can be expressed as in (11) and the control variable is the zero-sequence component within the defined range in (7). The sample within (7) which leads to the minimum value of (10) is the optimal zero-sequence signal in each switching period.

$$\begin{cases} \min J = \sum_{j=1}^3 \Delta v_{Cj} i_{Cj} = \sum_{j=1}^3 (v_{Cj} - \frac{V_{dc}}{3}) \cdot i_{Cj} \\ \text{Constraint: } -u_{\min}^*(t) \leq c(t) \leq 3 - u_{\max}^*(t) \end{cases} \quad (11)$$

The next step is to find the relationship between the control objective and zero-sequence signal so that each zero-sequence signal can be evaluated against the control objective. In (11), ΔV_{Cj} can be directly measured by the voltage sensor. Then, the key thing is to find the relationship between the capacitor current i_{Cj} and zero-sequence voltage $c(t)$. First, the relationship between capacitor current i_{Cj} in (11) and neutral point currents i_{N1} , i_{N2} can be derived according to Fig.6.

In Fig.6 (a), the converter output is clamped to N1 and the load current flows through the lower neutral point N1 (output voltage level E). Given the whole dc-link voltage is constant, the voltage change across C1 is equal to the total voltage change across C2 and C3. Therefore, the relationship between the neutral point current i_{N1} and capacitor current (i_{C1} , i_{C2} and i_{C3}) can be expressed as in (12).

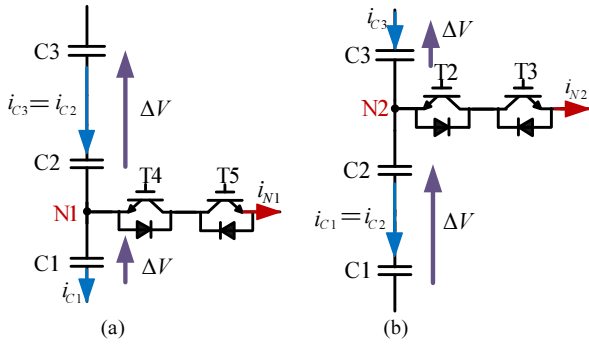


Fig.6. Relationship between capacitor currents and neutral currents (a) current flows through N1 (b) current flows through N2

$$\begin{cases} i_{C1} = -\frac{2}{3}i_{N1} \\ i_{C2} = \frac{1}{3}i_{N1} \\ i_{C3} = \frac{1}{3}i_{N1} \end{cases} \quad (12)$$

Then, combined with the condition where the current flows through the upper neutral point N2 as shown in Fig.6(b), the relationship between capacitors currents and neutral point currents can be established as in (13).

$$\begin{cases} i_{C1} = -\frac{1}{3}i_{N2} - \frac{2}{3}i_{N1} \\ i_{C2} = -\frac{1}{3}i_{N2} + \frac{1}{3}i_{N1} \\ i_{C3} = \frac{2}{3}i_{N2} + \frac{1}{3}i_{N1} \end{cases} \quad (13)$$

Next, the relationship between neutral currents (i_{N1} and i_{N2}) and zero-sequence signal $c(t)$ can be derived as follows. Since the p.u. value of the reference voltage has a range of 0~3, with any arbitrary value of the reference voltage, the integer part can represent the voltage level ($\text{int}(u_i)$), while the fractional part can determine the duty cycle ($\text{frac}(u_i)$). This significantly simplifies the calculation to find out the relationship between neutral point currents, modulation signals and phase currents. For example, when the reference voltage p.u. value is 1.2, then, the voltage level is 1 and the duty cycle is 0.2. In this case, the output

voltage will switch between E and 2E as illustrated in Fig.7. Specifically, the duty cycle for output voltage E is 80% with switches T4 and T5 ON, where the phase output current flows through N1. The duty cycle for output voltage 2E is 20% with switches T2 and T3 ON, where the phase current flows through N2. Therefore, neutral currents (i_{N1} , i_{N2}) can be determined by the reference voltage level ($\text{int}(u_i)$) and the duty cycle ($\text{frac}(u_i)$).

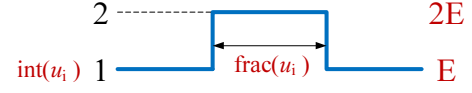


Fig.7. Illustration of the reference voltage level and duty cycle

Therefore, the relationship between the neutral point current and the reference voltage (after zero-sequence voltage injected) can be formulated as in (14) according to the method in [45-46].

$$\begin{cases} \bar{i}_{N1} = \sum_{i=a,b,c} i_i \times \left[\begin{aligned} &(\text{int}(u_i) == 0 \times \text{frac}(u_i) + \\ &(\text{int}(u_i) == 1) \times (1 - \text{frac}(u_i)) \end{aligned} \right] \\ \bar{i}_{N2} = \sum_{i=a,b,c} i_i \times \left[\begin{aligned} &(\text{int}(u_i) == 1 \times \text{frac}(u_i) + \\ &(\text{int}(u_i) == 2) \times (1 - \text{frac}(u_i)) \end{aligned} \right] \end{cases} \quad (14)$$

where, i_a , i_b , i_c are converter three-phase currents. $\text{int}(u_i) == 0$ is used to check whether the reference voltage level is 0 or not. If it is zero, then $(\text{int}(u_i) == 0)$ equals to 1, otherwise 0. It can be seen that only when the voltage level is 0 or 1, the phase current may flow through N1. When the voltage level is 1 or 2, the phase current will flow through N2. And the amount of current flows through neutral points will be determined by $\text{frac}(u_i)$. As the reference voltage u_i can be adjusted by the zero-sequence component, then, the relationship between zero-sequence component, the neutral current, the corresponding capacitor current and the control objective can be established through (6)-(14). Consequently, with an appropriate zero-sequence signal, the control objective can be achieved. Fig.8 presents the control algorithm in a flow chart.

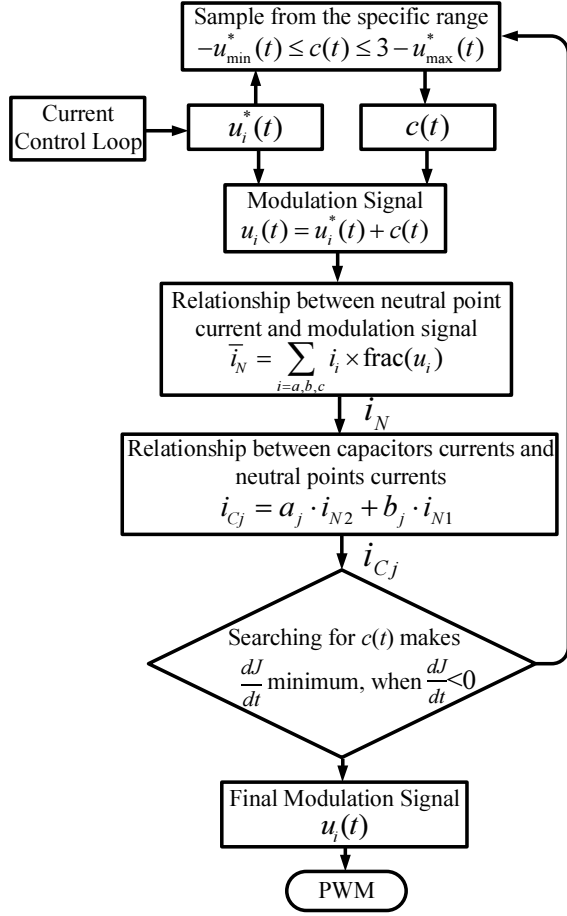


Fig.8. Neutral points' voltages balancing algorithm

Though the above control attempts to balance neutral point voltages, it can only achieve that under low modulation indices or low power factors when a single-end converter (inverter or rectifier) is used [4, 23]. From the carrier-based modulation point of view, higher modulation indices mean a smaller range of zero-sequence components can be selected. To overcome this limit, a back-to-back configuration is required as shown in Fig.9. With the presented control strategy above, the net current flowing into each neutral point from both sides can be controlled as close to zero as possible due to the symmetrical structure of the system, therefore achieving the neutral point voltage balance.

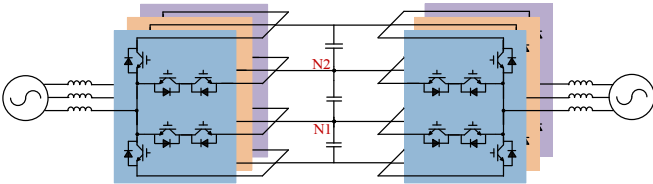


Fig.9. Back-to-back four-level π -type converter structure

V. POWER LOSS ANALYSIS AND EXPERIMENTAL RESULTS

A. Power Loss Analysis Results

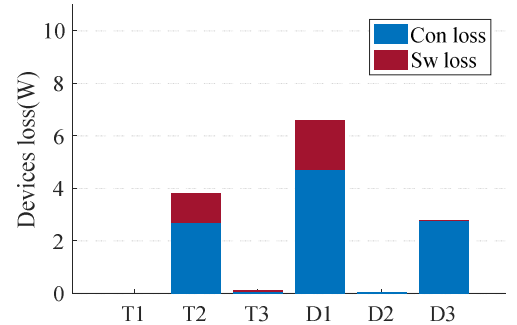
With the power loss model presented in Section III, the results can be obtained. Table III shows the selected devices

used in the calculation based on a 600V dc-link voltage. In theory, equations in (3) and (5) can be further derived analytically for each device. However, the analytical expression will be complicated. In this case, an equivalent piecewise numerical method is used to calculate the power loss in (3) and (5).

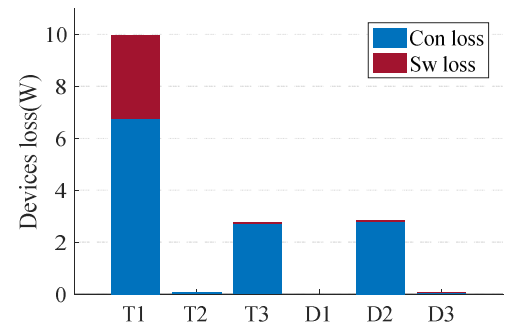
TABLE III. SELECTED IGBT DEVICES

Switch	Device
T1, T6	FGW15N120VD (1200V)
T2, T3, T4, T5	IKW30N60H3 (600V)

Fig.10 (a) (b) show the power loss distribution among various devices for a high modulation index with inverter and rectifier operating at 10 kHz switching frequency and 15A converter rated current. When the converter operates as a rectifier with a high modulation index ($m=0.95$), power losses generated in D1, T2, D3 are higher than that in D2, T3, T1. In comparison, when the converter operates in the inverter mode, losses generated in D2, T3 and T1 are higher than that in D1, T2, D3. Note only T1~T3, D1~D3 have been analyzed, as T4~T6, D4~D6 have the same averaged loss due to the symmetrical structure of the phase leg. Fig.10 (c) (d) show the converter efficiency variation with switching frequency for rectifier and inverter operations under $m=0.95$ in comparison with two-level and three-level (NPC and T-type) converters. In both operation modes, due to higher conduction loss (more devices in series in the conduction paths), the π -type converter shows a lower efficiency when the switching frequency is below 5 kHz. And the converter shows a higher efficiency when the switching frequency is above 5 kHz due to a lower switching losses.



(a) Rectifier mode ($m=0.95$) (Con: conduction, Sw: switching)



(b) Inverter mode ($m=0.95$)

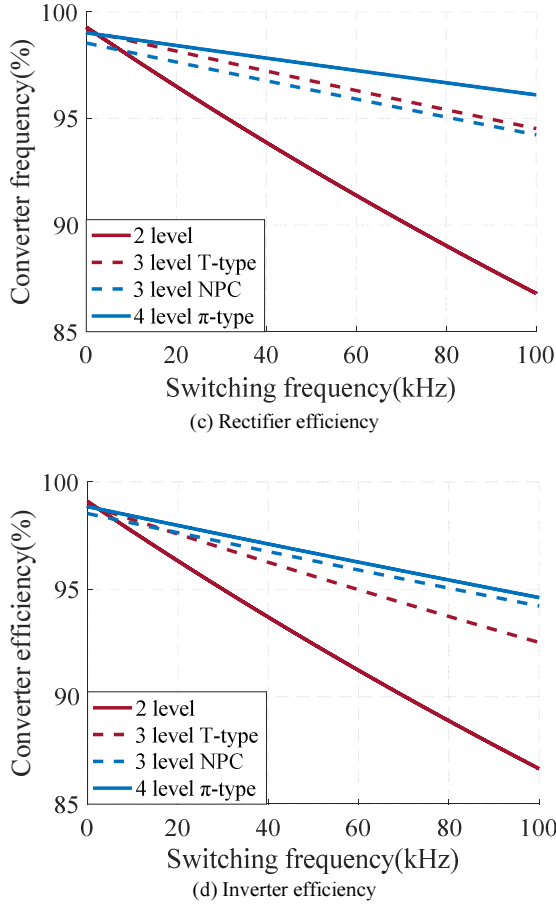


Fig.10. Power loss and efficiency using analytical loss models

B. Experimental Results

Using IGBTs in Table III, a four-level π -type converter prototype has been built. This prototype is designed for an output power of 3kW and allows the switching frequency to be set in a range from 5 kHz to 50 kHz with a nominal dc-link voltage of 600V.

The converter is controlled by a DSP-FPGA board which consists of a Xilinx SPARTAN XC3S400 FPGA and a TI TMS320 F28335 DSP. One part of the prototype (inverter) is shown in Fig.11.

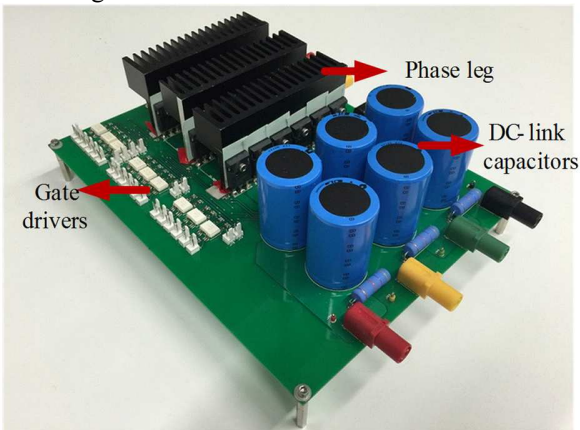
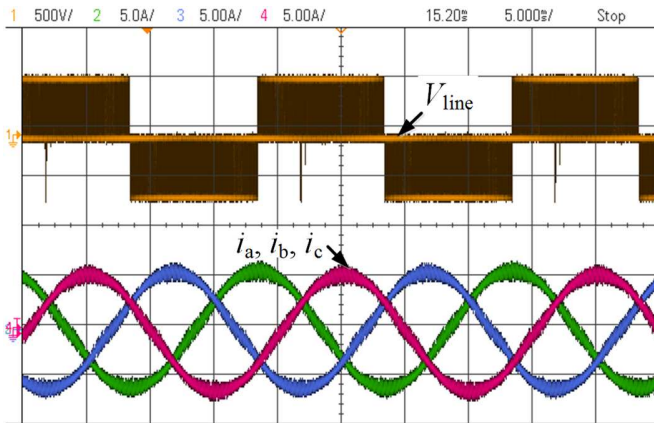


Fig.11. Experimental prototype of the four-level π -type inverter

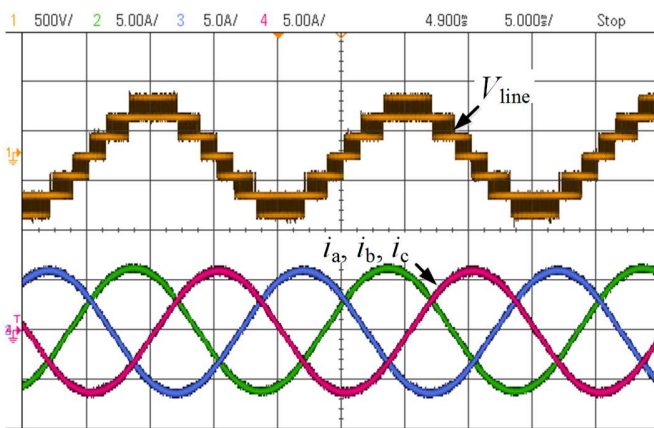
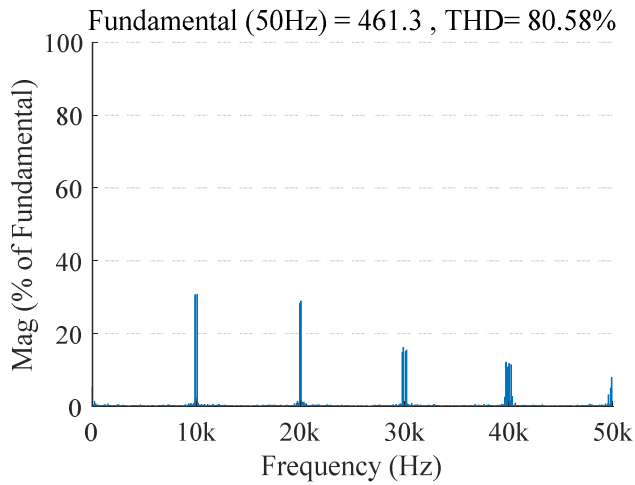
The input and output power of the four-level π -type inverter have been measured with two NORMA 4000 high bandwidth power analyzers (error limit between 0.03% and 0.3%). Measurements were conducted with a fixed RL load ($R=44\Omega$, $L=6.32\text{mH}$) and with a modulation index $m=0.95$. Three separate dc power supplies feed 200V voltage to three dc-link capacitors. Therefore, the total input dc-link voltage was fixed at 600V and a $2\mu\text{s}$ dead-time was used for all switches in order to prevent shoot-through. No forced cooling is applied.

To compare with a two-level converter, a two-level converter prototype based on FGW15N120VD (1200V) IGBTs is also built and tested. Fig.12 (a) (b) present the output waveforms of the two-level inverter and the four-level π -type inverter, respectively. The line voltage of the two-level inverter has three voltage levels, while that of the four-level π -type inverter has seven voltage levels as expected. The output current waveform of the two-level inverter is bolder than that of the four-level π -type, which means there are more high frequency harmonic components in two-level inverter output currents. Fig.12 (c) (d) show the harmonic analysis for line voltage waveforms in Fig.12 (a) (b), and Fig. 12 (e) (f) present the harmonic analysis for output current waveforms in Fig.12 (a) (b). Based on a 6.32mH inductor, the total harmonic distortion (THD) of the line voltage and output current of the four-level π -type inverter are 24.15% and 2.86%, respectively. While the THD of the line voltage and output current of the two-level inverter are 80.58% and 6.66%, respectively. Both aspects prove the four-level π -type inverter has much lower output harmonics, which means smaller filters are required than that of the two-level converter. Given the dead-time has not been compensated, the amount of decay on the actual output voltage depends on the duration of the deadtime, the switching frequency (switching period) and the switching voltage [47]. The decay on fundamental components in Fig.12 (c) (e) is higher than that in Fig.12 (d) (f), which means the dead-time will have less effect on the four-level π -type inverter due to a smaller switching voltage.

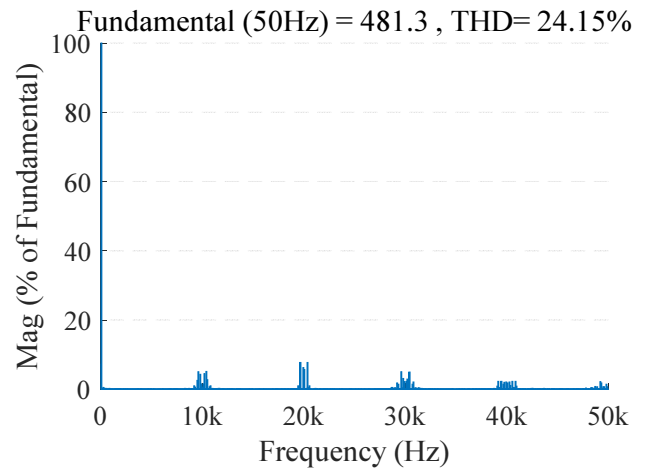
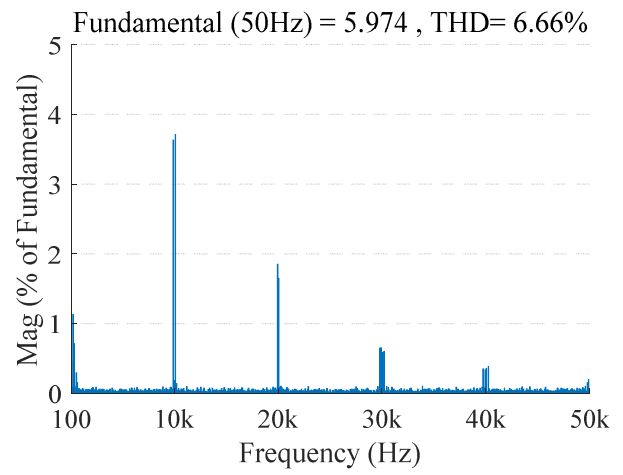
Fig.12 (g) shows the efficiency measurement for both the four-level π -type inverter and two-level inverter for comparison. The experimental efficiency agrees with analytical predictions reasonably well, which validates the presented power loss model and proves the four-level π -type inverter has the higher efficiency than the two-level converter at higher switching frequencies as expected. Fig.12 (h) sets the frequency axis as log axis in order to show the cross point clearer.



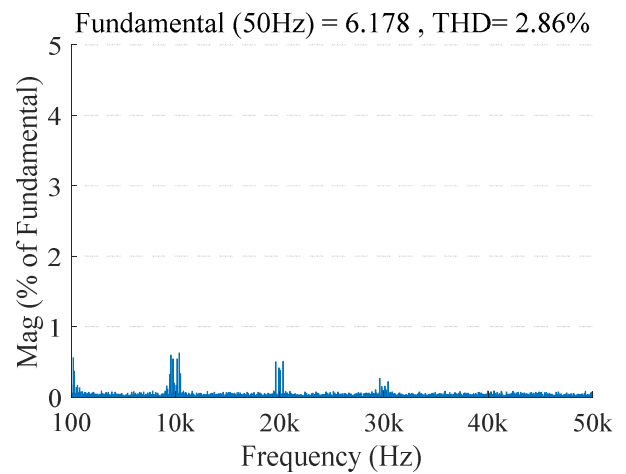
(a) Two-level inverter output waveforms

(b) Four-level π -type inverter output waveforms

(c) Line voltage harmonics of the two-level inverter

(d) Line voltage harmonics of the four-level π -type inverter

(e) Output current harmonics of the two-level inverter

(f) Output current harmonics of the four-level π -type inverter

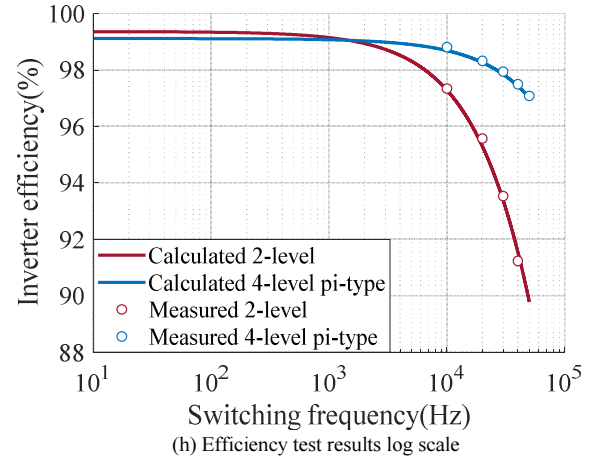
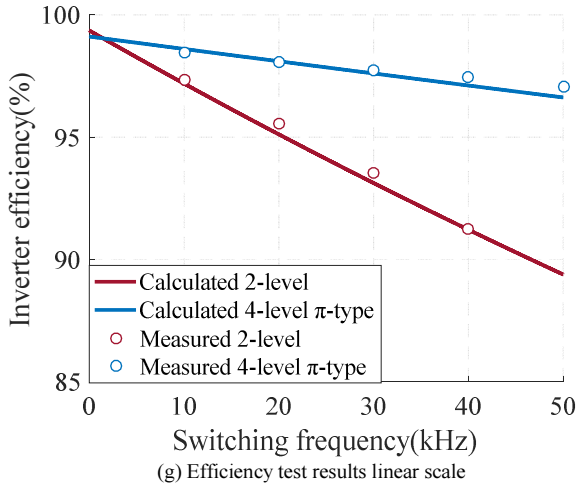


Fig.12. Experimental results of harmonic analysis and efficiency.

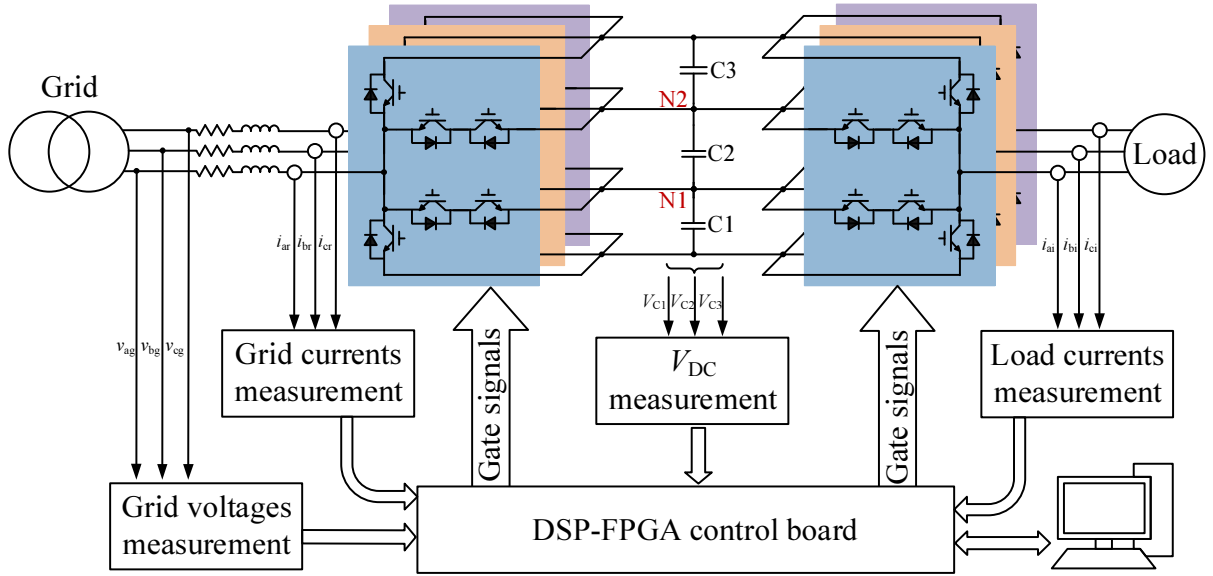


Fig.13. Diagram of the back-to-back four-level π -type converter test prototype

To validate the neutral points voltage control with a back-to-back configuration, two converters as shown in Fig.11 are linked together through the dc-link. They are controlled together by one control board. The diagram of the back-to-back configuration is shown in Fig.13. The test setup includes a three-phase 5mH choke (equivalent resistance 0.2Ω) at the input of the rectifier and a three-phase star-connected resistance-inductance load ($R=21\Omega$, $L=6.32\text{mH}$) at the inverter output. Power factors on both sides are close to 1 (unity power factor condition, the worst-case scenario). The dc-link voltage is set as 300V. The value of each dc-link capacitor is $1000\mu\text{F}$. Fundamental frequencies and switching frequencies on both sides are 50 Hz and 10 kHz, respectively. At the rectifier/grid side, a dc-link voltage loop and a current loop are used with PI controllers. An open loop voltage control is applied to the

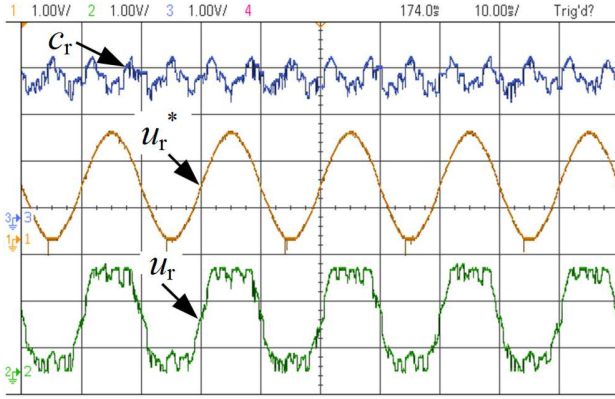
inverter side. The dc-link neutral points voltage balancing control is employed on both sides.

Fig.14 presents converter operation waveforms with $m_{\text{rec}}=m_{\text{inv}}=1.1$ (same modulation indices on both sides). Here, the modulation index is defined as the peak of the fundamental sinusoidal modulation wave divided by the peak of the carrier waveform. Hence, $m=1$ represents the maximum modulation index that a standard SPWM can achieve without zero-sequence voltage injection. Using an AD5725 DAC chip, internal variables in the program can be monitored. Modulation waveforms as well as injected zero-sequence signal waveforms on both sides are shown in Fig.14 (a) (b). Yellow waveforms represent fundamental components (u_r^*) which are sinusoidal. Blue waveforms are the selected zero-sequence components (C_i), and their frequencies are triples of the fundamental

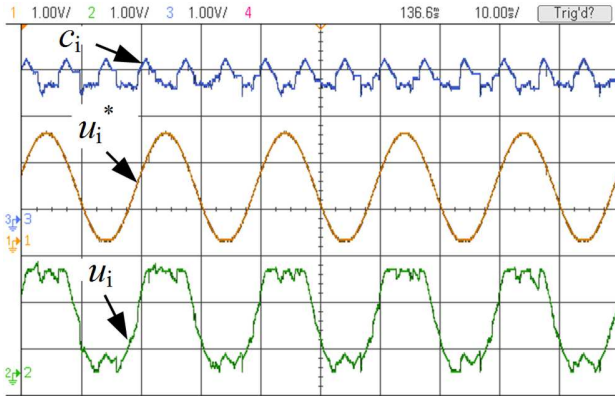
components. Green waveforms are final modulation signals by combining previous two waveforms.

Fig. 14 (c) shows the rectifier ac-side phase voltage as well as the line voltage. Under a 1.1 modulation index, the phase voltage has four levels and the line voltage has seven levels as expected. Inverter voltage waveforms in Fig. 14 (d) have the same features as the rectifier side ones have. Fig. 14 (e) (f) show rectifier and inverter ac-side three-phase sinusoidal currents.

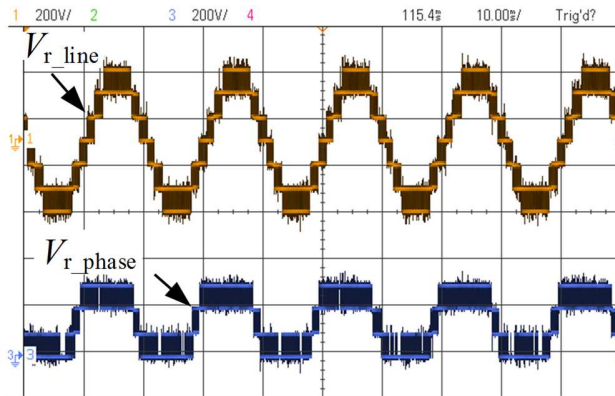
Fig. 14 (g) presents three dc-link capacitors' voltages. As expected, capacitor voltages are well balanced by the control method presented in Section IV. In order to present these voltages more clearly, offsets of three oscilloscope channels are set differently in Fig. 14 (h) to present these three voltages.



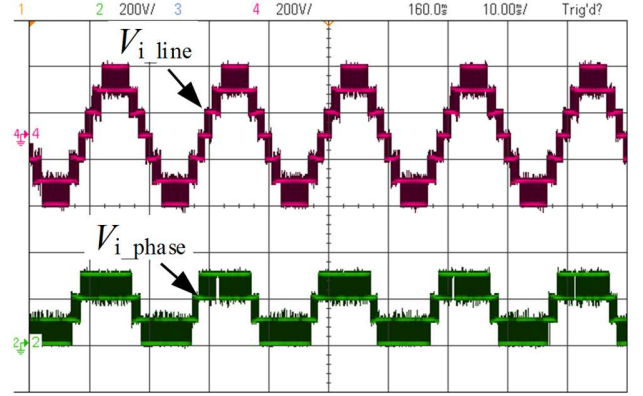
(a) Rectifier modulation and zero-sequence signals



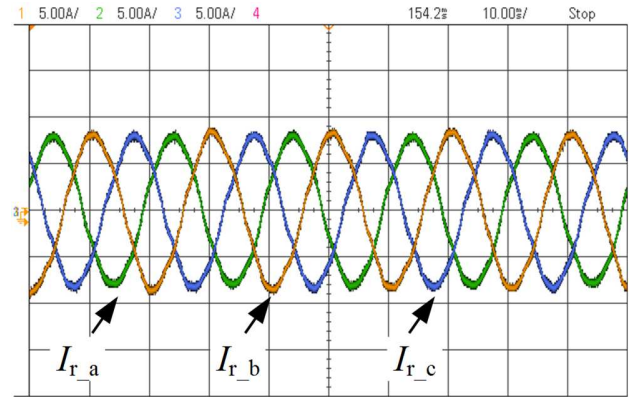
(b) Inverter modulation and zero-sequence signals



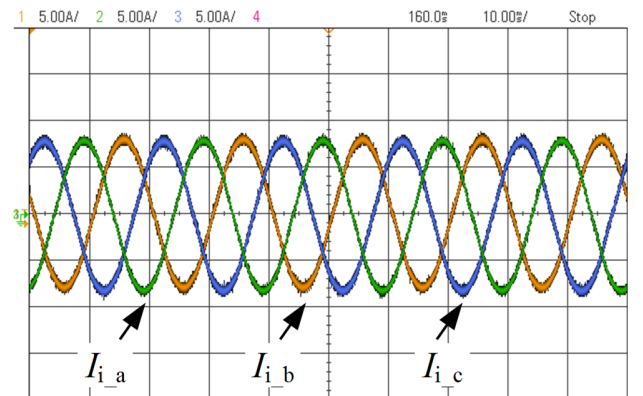
(c) Rectifier output phase and line voltages



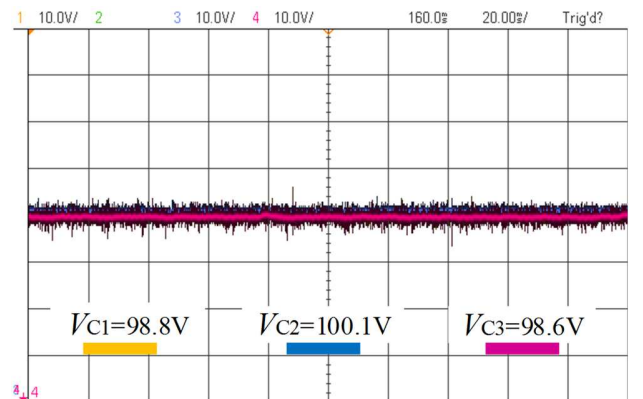
(d) Inverter output phase and line voltages



(e) Rectifier ac side three-phase currents



(f) Inverter ac side three-phase currents



(g) dc-link capacitors' voltages

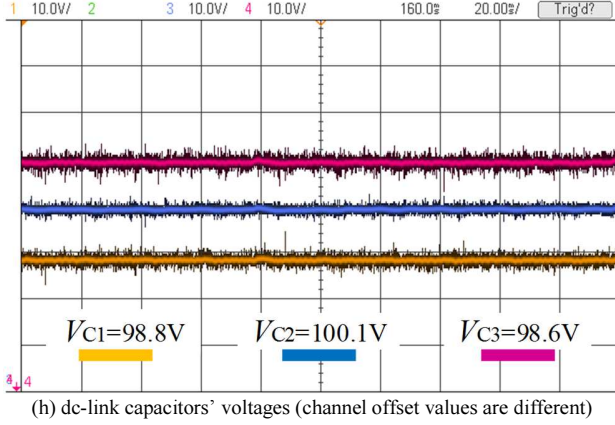
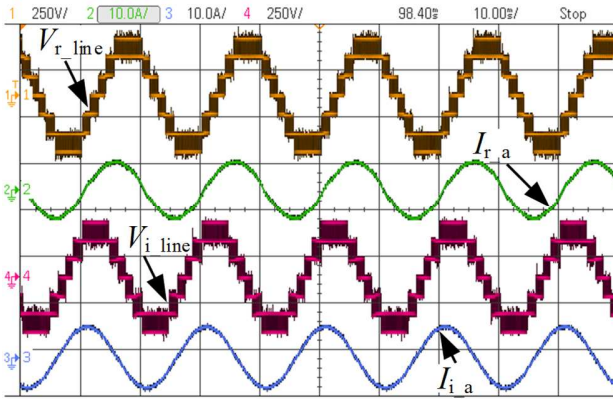


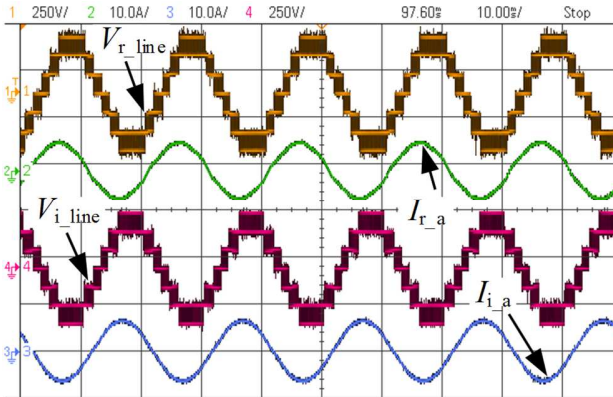
Fig.14. Experimental results with the same modulation indices (1.1) on each side

The scenarios with different modulation indices on the rectifier side and inverter side have also been tested in order to verify the dc-link capacitor voltage fully controllable region of

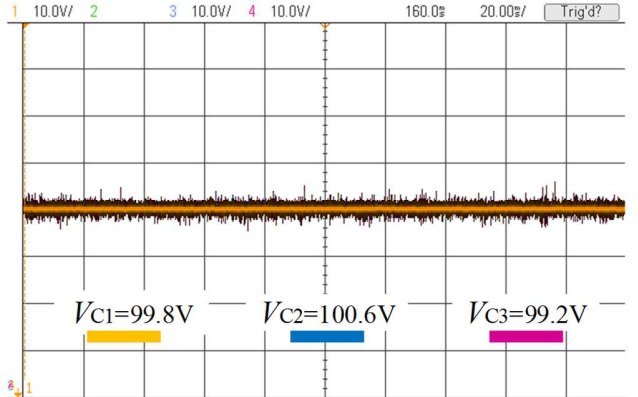
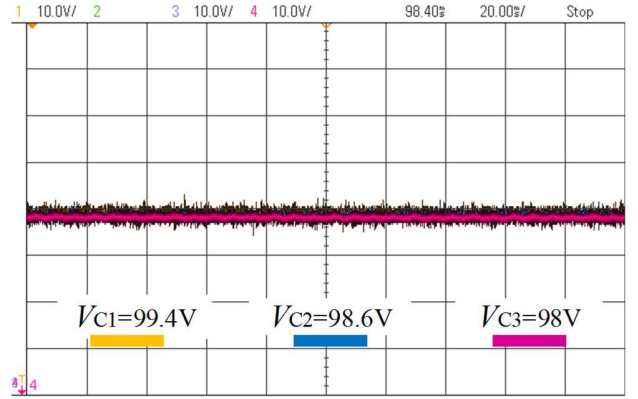
the back-to-back configuration under the unity power factor operation. Fig.15 (a) presents the condition of $m_{rec}=1.05$ and $m_{inv}=1.06$, where modulation indices on both sides are close, and three dc-link capacitor voltages can be well balanced. Fig.15 (b) presents the condition of $m_{rec}=1.05$ and $m_{inv}=1.02$, where modulation indices on both sides are close as well, but m_{inv} is slightly lower than m_{rec} . Three dc-link capacitors can be well balanced. Fig.15 (c) presents the condition of $m_{rec}=1.05$ and $m_{inv}=0.7$, where modulation indices have clear difference. The rectifier line voltage has seven levels while the inverter line voltage only has five levels due to a lower modulation index. Given the same power transfer, the rectifier current is lower than the inverter current. The three dc-link capacitor voltages are still balanced. Fig.15 (d) and (e) show another two conditions where the voltage balance can be achieved. Fig.15 (f) presents the condition of $m_{rec}=1.1$ and $m_{inv}=0.75$, where the middle capacitor discharges completely, causing unbalanced capacitor voltages. Fig.15 (g) shows another unbalanced condition of $m_{rec}=1.05$ and $m_{inv}=0.95$.

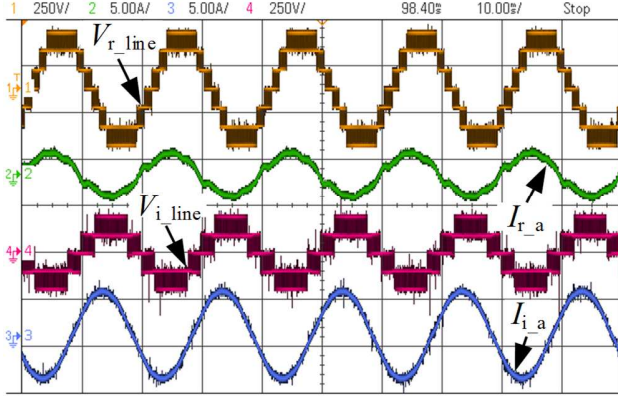
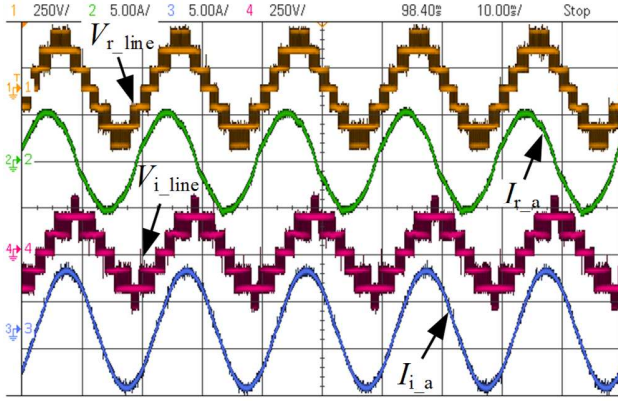
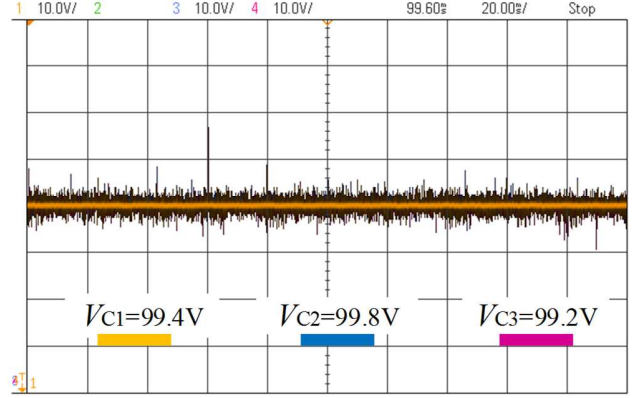
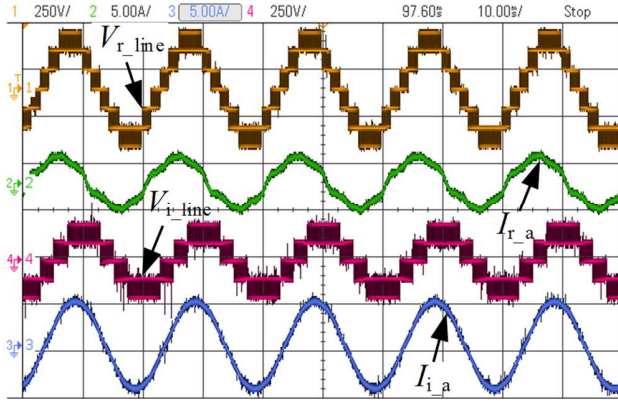
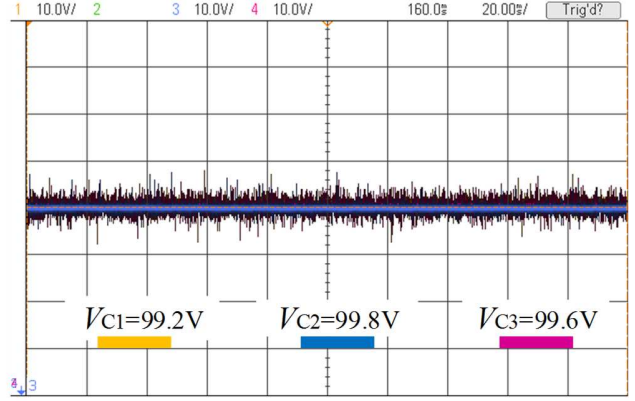
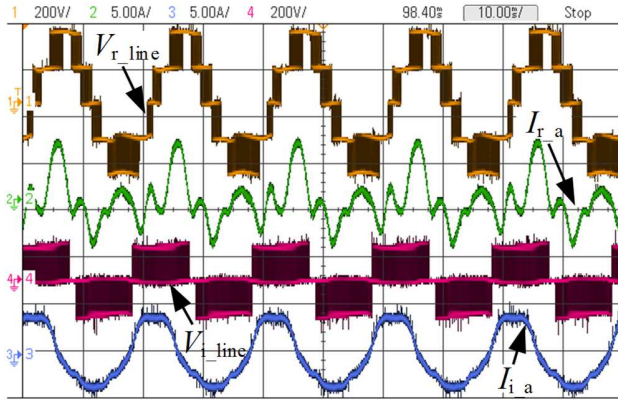
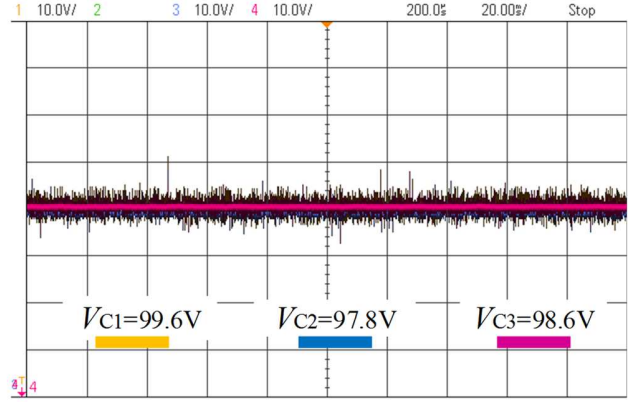
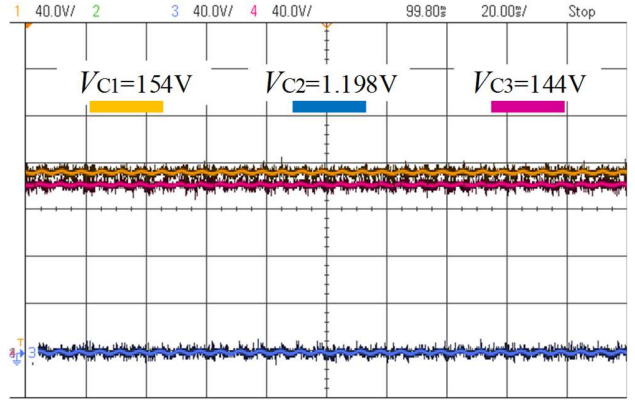


(a) $m_{rec}=1.05$, $m_{inv}=1.06$



(b) $m_{rec}=1.05$, $m_{inv}=1.02$



(c) $m_{rec}=1.05$, $m_{mv}=0.7$ (d) $m_{rec}=0.9$, $m_{mv}=0.8$ (e) $m_{rec}=0.95$, $m_{mv}=0.6$ (f) $m_{rec}=1.1$, $m_{mv}=0.75$ 

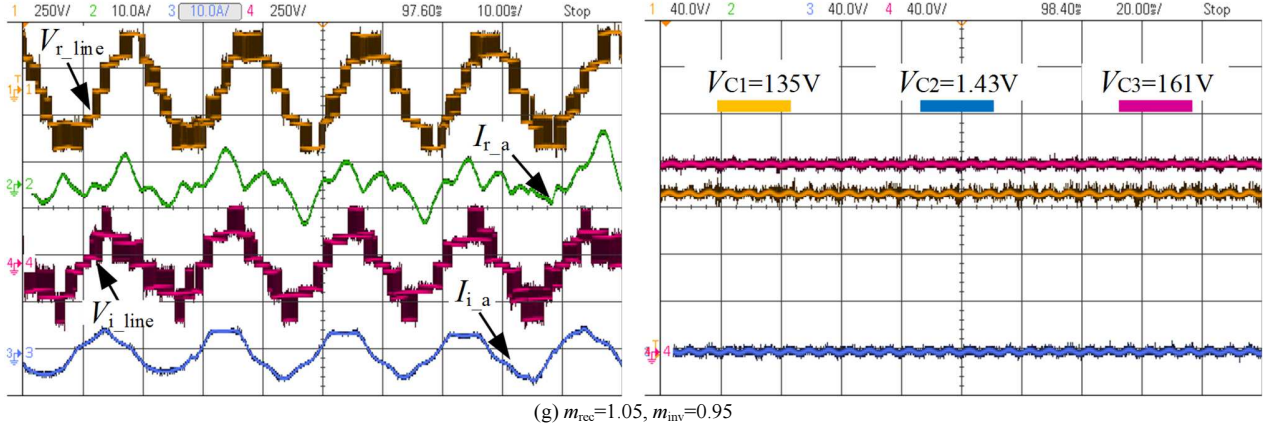


Fig. 15. Experimental results with different modulation indices on each side under unity power factor operation: Line voltage and current of both sides; three dc-link capacitor voltages.

Based on extensive experimental measurements, Fig.16 summaries the dc-link capacitor voltage balanceable and unbalanceable region under the unity power factor condition with the back-to-back structure. The test condition shown in Fig.15 have also been highlighted in the figure. As seen, generally, dc-link capacitor voltages are more difficult to balance under high modulation indices. However, closer modulation indices at both sides help to balance the voltages.

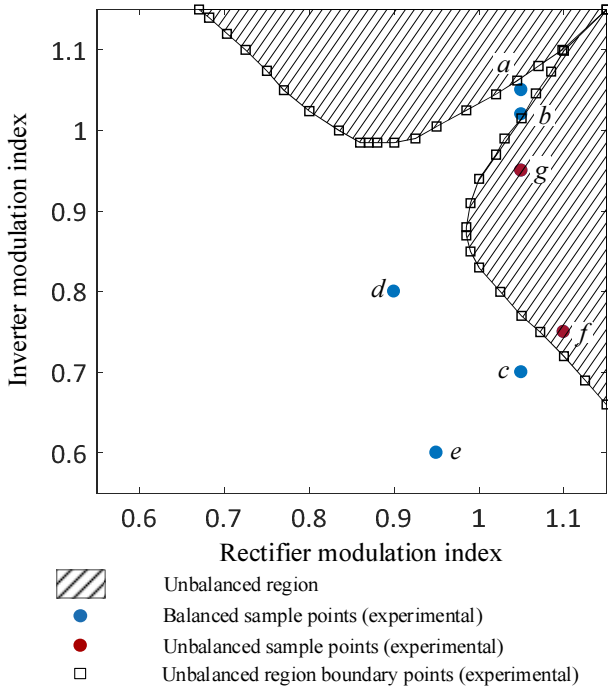


Fig. 16. Balanced and unbalanced region based on experimental measurements under unity power factor operation on both sides

VI. CONCLUSIONS

This paper has presented the topology, power loss analysis and control of a four-level π -type converter, which can be a good candidate for low voltage applications in terms of reduced harmonic components and switching loss. With common collector connection of the IGBTs in the neutral paths, this

topology only requires two additional gate driver power supplies compared with the standard two-level converter. The modulation process for the four-level π -type converter can be greatly simplified compared with the conventional space vector modulation with the level shift carrier-based modulation. The four-level π -type converter shows higher efficiency than two-level and three-level converters at switching frequencies higher than 5 kHz due to reduced switching loss. In addition, the neutral point voltage drift issue can be resolved by adopting the presented LS carrier-based optimal zero-sequence injection voltage balancing control and a back-to-back configuration. The experiment has validated this control strategy where the three dc-link capacitor voltages can be well controlled even under high modulation indices and high power factors. The fully balanceable region for the back-to-back configuration under unity power factor condition has been presented.

APPENDIX

A. Conduction Intervals

TABLE A.I $M > \frac{1}{3}$, $\phi \leq \sin^{-1}(\frac{1}{3M})$

Device	Conduction intervals
T1	$[\sin^{-1}(\frac{1}{3M}), \pi - \sin^{-1}(\frac{1}{3M})]$
D1	Null
T2	$[0, \phi]$, $[\pi + \phi, \pi + \sin^{-1}(\frac{1}{3M})]$, $[2\pi - \sin^{-1}(\frac{1}{3M}), 2\pi]$
D2	$[\phi, \sin^{-1}(\frac{1}{3M})]$, $[\sin^{-1}(\frac{1}{3M}), \pi - \sin^{-1}(\frac{1}{3M})]$, $[\pi - \sin^{-1}(\frac{1}{3M}), \pi + \phi]$
T3	$[\phi, \sin^{-1}(\frac{1}{3M})]$, $[\sin^{-1}(\frac{1}{3M}), \pi - \sin^{-1}(\frac{1}{3M})]$, $[\pi - \sin^{-1}(\frac{1}{3M}), \pi + \phi]$
D3	$[0, \phi]$, $[\pi + \phi, \pi + \sin^{-1}(\frac{1}{3M})]$, $[2\pi - \sin^{-1}(\frac{1}{3M}), 2\pi]$

TABLE A.II $M > \frac{1}{3}$, $\sin^{-1}(\frac{1}{3M}) < \phi < \pi - \sin^{-1}(\frac{1}{3M})$

Device	Conduction intervals
T1	$[\phi, \pi - \sin^{-1}(\frac{1}{3M})]$
D1	$[\sin^{-1}(\frac{1}{3M}), \phi]$
T2	$[0, \sin^{-1}(\frac{1}{3M})]$, $[\sin^{-1}(\frac{1}{3M}), \phi]$, $[2\pi - \sin^{-1}(\frac{1}{3M}), 2\pi]$
D2	$[\phi, \pi - \sin^{-1}(\frac{1}{3M})]$, $[\pi - \sin^{-1}(\frac{1}{3M}), \pi + \sin^{-1}(\frac{1}{3M})]$
T3	$[\phi, \pi - \sin^{-1}(\frac{1}{3M})]$, $[\pi - \sin^{-1}(\frac{1}{3M}), \pi + \sin^{-1}(\frac{1}{3M})]$
D3	$[0, \sin^{-1}(\frac{1}{3M})]$, $[\sin^{-1}(\frac{1}{3M}), \phi]$, $[2\pi - \sin^{-1}(\frac{1}{3M}), 2\pi]$

TABLE A.III. $M > \frac{1}{3}$, $\Pi - \sin^{-1}(\frac{1}{3M}) \leq \phi < \Pi$

Device	Conduction intervals
T1	Null
D1	$[\sin^{-1}(\frac{1}{3M}), \pi - \sin^{-1}(\frac{1}{3M})]$
T2	$[0, \sin^{-1}(\frac{1}{3M})], [\sin^{-1}(\frac{1}{3M}), \pi - \sin^{-1}(\frac{1}{3M})], [\pi - \sin^{-1}(\frac{1}{3M}), \phi], [\phi + \pi, 2\pi]$
D2	$[\phi, \pi + \sin^{-1}(\frac{1}{3M})], [2\pi - \sin^{-1}(\frac{1}{3M}), \phi + \pi]$
T3	$[\phi, \pi + \sin^{-1}(\frac{1}{3M})], [2\pi - \sin^{-1}(\frac{1}{3M}), \phi + \pi]$
D3	$[0, \sin^{-1}(\frac{1}{3M})], [\sin^{-1}(\frac{1}{3M}), \pi - \sin^{-1}(\frac{1}{3M})], [\pi - \sin^{-1}(\frac{1}{3M}), \phi], [\phi + \pi, 2\pi]$

TABLE A.IV. $M \leq \frac{1}{3}$

Device	Conduction intervals
T1	Null
D1	Null
T2	$[0, \phi], [\pi + \phi, 2\pi]$
D2	$[\phi, \pi + \phi]$
T3	$[\phi, \pi + \phi]$
D3	$[0, \phi], [\pi + \phi, 2\pi]$

B. Switching Intervals

TABLE B.I. $M > \frac{1}{3}$, $\phi \leq \sin^{-1}(\frac{1}{3M})$

Device	Switching intervals
T1	$[\sin^{-1}(\frac{1}{3M}), \pi - \sin^{-1}(\frac{1}{3M})]$
D1	Null
T2	Null
D2	$[\sin^{-1}(\frac{1}{3M}), \pi - \sin^{-1}(\frac{1}{3M})]$
T3	$[\phi, \sin^{-1}(\frac{1}{3M})], [\pi - \sin^{-1}(\frac{1}{3M}), \pi + \phi]$
D3	$[0, \phi], [\pi + \phi, \pi + \sin^{-1}(\frac{1}{3M})], [2\pi - \sin^{-1}(\frac{1}{3M}), 2\pi]$

TABLE B.II. $M > \frac{1}{3}$, $\sin^{-1}(\frac{1}{3M}) < \phi < \Pi - \sin^{-1}(\frac{1}{3M})$

Device	Switching intervals
T1	$[\phi, \pi - \sin^{-1}(\frac{1}{3M})]$
D1	$[\sin^{-1}(\frac{1}{3M}), \phi]$
T2	$[\sin^{-1}(\frac{1}{3M}), \phi]$
D2	$[\phi, \pi - \sin^{-1}(\frac{1}{3M})]$
T3	$[\pi - \sin^{-1}(\frac{1}{3M}), \pi + \sin^{-1}(\frac{1}{3M})]$
D3	$[0, \sin^{-1}(\frac{1}{3M})], [2\pi - \sin^{-1}(\frac{1}{3M}), 2\pi]$

TABLE B.III. $M > \frac{1}{3}$, $\Pi - \sin^{-1}(\frac{1}{3M}) \leq \phi < \Pi$

Device	Switching intervals
T1	Null
D1	$[\sin^{-1}(\frac{1}{3M}), \pi - \sin^{-1}(\frac{1}{3M})]$
T2	$[\sin^{-1}(\frac{1}{3M}), \pi - \sin^{-1}(\frac{1}{3M})]$
D2	Null
T3	$[\phi, \pi + \sin^{-1}(\frac{1}{3M})], [2\pi - \sin^{-1}(\frac{1}{3M}), \phi + \pi]$
D3	$[0, \sin^{-1}(\frac{1}{3M})], [\pi - \sin^{-1}(\frac{1}{3M}), \phi], [\phi + \pi, 2\pi]$

TABLE B.IV. $M \leq \frac{1}{3}$

Device	Switching intervals
T1	Null
D1	Null
T2	Null
D2	Null
T3	$[\phi, \pi + \phi]$
D3	$[0, \phi], [\pi + \phi, 2\pi]$

REFERENCES

- [1] M. Schweizer, J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electronics*, vol. 28, no.2, pp. 899-907, Feb. 2013.
- [2] K. Wang, Z. Zheng, L. Xu, Y. Li, "A four-level hybrid-clamped converter with natural capacitor voltage balancing ability," *IEEE Trans. Power Electronics*, vol. 29, no.3, pp. 1152-1162, Mar. 2014.
- [3] B. Wang, "Four-level neutral point clamped converter with reduced switch count," in *Proc. IEEE PESC'08 Conf.*, pp. 2626-2632, Aug 2008.
- [4] J. Pou, R. Pindado, D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Trans. Industrial Electronics*, vol. 52, no.1, pp. 190-196, Feb. 2005.
- [5] I. Hasegawa, S. Urushibata, T. Kondo, K. Hirao, "Back-to-back system for five-level converter with common flying capacitors," in *Proc. IEEE IPEC'14 Conf.*, pp. 1-6, Aug. 2014.
- [6] Z. Pan, F. Peng, "A sinusoidal PWM method with voltage balancing capability for diode-clamped five-Level converters," *IEEE Trans. Industry Application*, vol. 45, no.3, pp. 1028-1034, May. 2009.
- [7] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, "Active neutral-point-clamped multilevel converters," in *Proc. IEEE PESC'05 Conf.*, pp. 2296-2301, Jun. 2005.
- [8] X. Yuan, "Analytical averaged loss model of a three-level T-type converter," in *Proc. IET PEMD'14 Conf.*, pp. 1-6, Jun. 2014.
- [9] B. Jin, X. Yuan, "Power loss and efficiency analysis of a four-level π -type converter," in *Proc. EPE'15 Conf.*, pp. 1-10, Oct. 2015.
- [10] P. Bhagwat, V. Stefanovic, "Generalized structure of a multilevel pwm inverter," *IEEE Trans. Industry Application*, vol. 19, no.6, pp. 1057-1069, Nov. 1983.
- [11] E. Babaei, S.H. Hosseini, G.B. Gharehpetian, M. TarafdarHaque, M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," *Electr. Power Syst. Res.*, vol. 77, no.8, pp. 1073-1085, Jun. 2007.
- [12] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electronics*, vol. 23, no.6, pp. 2657-2664, Nov. 2008.
- [13] K. Gupta, A. Ranjan, P. Bhatnagar, L. Sahu, S. Jain, "Multilevel inverter topologies with reduced device count: a review," *IEEE Trans. Power Electronics*, vol. 31, no.1, pp. 135-151, Jan. 2016.
- [14] X. Yuan, "Derivation of voltage source multilevel converter topologies," *IEEE Trans. Industrial Electronics*, vol. 64, no.2, pp. 966-976, Feb. 2016.
- [15] Y. Xue, M. Manjrekar, "A new class of single-phase multilevel inverters," in *Proc. PEDGS'10 Conf.*, pp. 565-571, Jun. 2010.
- [16] A. Khoshkbar Sadigh, M. Abarzadeh, K. Corzine, V. Dargahi, "A new breed of optimized symmetrical and asymmetrical cascaded multilevel power converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no.4, pp. 1160-1170, Dec. 2015.
- [17] X. Yuan, "A four-level π -type converter for low-voltage applications," in *Proc. EPE'15 Conf.*, pp. 1-9, Oct. 2015.
- [18] Z. Pan, F. Z. Peng, "Harmonics optimization of the voltage balancing control for multilevel converter/inverter systems," *IEEE Trans. Power*

- Electronics*, vol. 21, no.1, pp. 211-218, Jan. 2006.
- [19] M. Marchesoni, P. Tenca, "Diode-clamped multilevel converters a practicable way to balance DC-link voltages," *IEEE Trans. Industrial Electronics*, vol. 49, no.4, pp. 752-765, Aug. 2002.
- [20] M. Marchesoni, P. Tenca, "Theoretical and practical limits in multi-level MPC inverters with passive front ends," in *Proc. EPE'01 Conf.*, pp. 1-12, Apr. 2001.
- [21] Z. Pan, F. Z. Peng, K.A. Corzine, V.R. Stefanovic, J.M. Leuthen, S. Gataric, "Voltage balancing control of diode-clamped multi-level rectifier/inverter systems," *IEEE Trans. Industrial Applications*, vol. 41, no.6, pp. 1698-1706, Dec. 2005.
- [22] M. Saeedifard, R. Iravani, J. Pou, "Analysis and control of DC-capacitor-voltage-drift phenomenon of a passive front-end five-level converter," *IEEE Trans. Industrial Electronics*, vol. 54, no.6, pp. 3255-3266, Dec. 2007.
- [23] M. Saeedifard, R. Iravani, J. Pou, "A space vector modulation strategy for a back-to-back five-level HVDC converter system," *IEEE Trans. Industrial Electronics*, vol. 56, no.2, pp. 452-466, Feb. 2009.
- [24] S. Busquets-Monge, A. Ruderman, "Carrier-based pwm strategies for the comprehensive capacitor voltage balance of multilevel multileg diode-clamped converters," in *Proc. IEEE ISIE'10 Conf.*, pp. 688-693, Jul. 2010.
- [25] M. Marchesoni, M. Mazzucchelli, "Extending the operating range in diode-clamped multilevel inverters with active front ends," in *Proc. IEEE IECE'12 Conf.*, pp. 63-68, Sept. 2012.
- [26] P. Fazio, G. Maragliano, M. Marchesoni, L. Vaccaro, "A new capacitor balancing technique in diode-clamped multilevel converters with active front end for extended operation range," in *Proc. IEEE EPE'11 Conf.*, pp. 1-10, Sept. 2011.
- [27] M. Mazuela, I. Baraia, A. Sanchez-Ruiz, I. Echeverria, I. Torre, I. Atutxa, "DC-link voltage balancing strategy based on svm and reactive power exchange for a 5L-MPC back-to-back converter for medium-voltage drives," *IEEE Trans. Industrial Electronics*, vol. 63, no.12, pp. 7864-7875, Dec. 2016.
- [28] S. Busquets-Monge, S. Alepuz, J. Bordonau, J. Peracaula, "Voltage balancing control of diode-clamped multilevel converters with passive front-ends," *IEEE Trans. Power Electronics*, vol. 23, no.4, pp. 1751-1758, Jul. 2008.
- [29] S. Busquets-Monge, J. Bordonau, J. Rocabert, "A virtual-vector pulsewidth modulation for the four-Level diode-clamped dc-ac converter," *IEEE Trans. Power Electronics*, vol. 23, no.4, pp. 1964-1972, Jul. 2008.
- [30] S. Busquets-Monge, S. Alepuz, J. Rocabert, J. Bordonau, "Pulsewidth modulations for the comprehensive capacitor voltage balance of n-level three-leg diode-clamped converters," *IEEE Trans. Power Electronics*, vol. 24, no.5, pp. 1364-1375, May. 2009.
- [31] S. Busquets-Monge, R. Maheshwari, J. Nicolas-Apruzzese, E. Lupon, S. Munk-Nielsen, J. Bordonau, "Enhanced dc-Link capacitor voltage balancing control of dc-ac multilevel multileg converters," *IEEE Trans. Industrial Electronics*, vol. 62, no.5, pp. 2663-2672, May. 2015.
- [32] G. Sinha, T. A. Lipo, "A four-level inverter based drive with a passive front end," *IEEE Trans. Power Electronics*, vol. 15, no.2, pp. 285-294, Mar. 2000.
- [33] M. Saeedifard, R. Iravani, J. Pou, "A space vector modulation approach for a back-to-back connected four-level converter," in *Proc. IEEE PESC'07 Conf.*, pp. 2043-2049, Oct. 2007.
- [34] F. Wang, "Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters," *IEEE Trans. Industry Applications*, vol. 38, no.2, pp. 500-506, Aug. 2002.
- [35] X. Yuan, Y. Li, C. Wang, "Objective optimisation for multilevel neutral-point-clamped converters with zero-sequence signal control," *IET Power Electronics*, vol. 3, no.5, pp. 755-763, Sept. 2010.
- [36] F. Grigoletto, H. Pinheiro, "Generalised pulse width modulation approach for dc capacitor voltage balancing in diode-clamped multilevel converters," *IET Power Electronics*, vol. 4, no.1, pp. 89-100, Sept. 2011.
- [37] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Trans. Industry Applications*, vol. 33, no.3, pp. 756-764, Aug. 2002.
- [38] B. Jin, X. Yuan, "Neutral points voltage balancing control of a four-level π -type converter," in *Proc. IEEE ECCE'16 Conf.*, pp. 1-8, Feb. 2017.
- [39] J. Pou, R. Pindado, D. Borayevich, P. Rodriguez, "Limits of the neutral-point balance in back-to-back connected three-level converters," *IET Power Electronics*, vol. 19, no.3, pp. 722-731, May. 2004.
- [40] T. Kim, D. Kang, Y. Lee, D. Hyun, "The analysis of conduction and switching losses in multi-level inverter system," in *Proc. IEEE PESC'01 Conf.*, vol.3, pp. 1363-1368, Aug. 2001.
- [41] S. Dieckerhoff, S. Bernet, D. Krug, "Power loss-oriented evaluation of high voltage IGBTs and multilevel converters in transformerless traction applications," *IEEE Trans. Power Electronics*, vol. 20, no.6, pp. 1328-1336, Nov. 2005.
- [42] www.fujielectric-europe.com/downloads/FGW15N120VD_1735030.PDF
- [43] www.infineon.com/dgdl/Infineon-IKW30N60H3-DS-v02_02-en.pdf?fileId=db3a3043266237920126bc80c5f041c9
- [44] M. Marchesoni, M. Mazzucchelli, P. Tenca, "An optimal controller for voltage balance and power losses reduction in MPC AC/DC/AC converters," in *Proc. IEEE PESC'00 Conf.*, vol.2, pp. 662-667, Aug. 2002.
- [45] S. Ogasawara, H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *Proc. IEEE IAS'93 Conf.*, pp. 965-970, Oct. 1993.
- [46] C. Wang, Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral point potential balancing in three-level NPC converters," *IEEE Trans. Industrial Electronics*, vol. 57, no.7, pp. 2262-2271, Jul. 2010.
- [47] A. C. Oliveira, C. B. Jacobina, and A. M. N. Lima, "Improved dead-time compensation for sinusoidal PWM inverters operating at high switching frequencies," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2295-2304, Aug. 2007.



Bosen Jin received the B.S. degree from Northumbria University, Newcastle, UK and the MSc degree from University College London, London, UK, in 2012 and 2013, respectively, both in electrical engineering. He is currently perusing the Ph.D degree at the Electrical Energy Management Group, Department of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K. His research interests include multilevel converter topologies, control and power loss analysis.



Xibo Yuan (S'09-M'11-SM'15) received the B.S. degree from China University of Mining and Technology, Xuzhou, China, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2005 and 2010, respectively, both in electrical engineering. He has been a Professor since 2017 in the Electrical Energy Management Group, Department of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K. He also holds the Royal Academy of Engineering/Safran Chair in Advanced Aircraft Power Generation Systems. He was a Visiting Scholar at the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, and the Institute of Energy Technology, Aalborg University, Denmark. He was a Postdoctoral Research Associate in the Electrical Machines and Drives Research Group, University of Sheffield, Sheffield, U.K.

His research interests include power electronics and motor drives, wind power generation, multilevel converters, application of wide-bandgap devices, electric vehicles and more electric aircraft technologies. Professor Yuan is an Associate Editor of IEEE Transactions on Industry Applications and IEEE Journal of Emerging and Selected Topics in Power Electronics. He is a Fellow of IET and received The Isao Takahashi Power Electronics Award in 2018.